Reference No.:	72
Project Title:	Evaluation of Three Dimensional Devices and Technologies
NEPP Project:	Electronics Packaging Project
Point of Contact:	Harry Shaw, GSFC, 301-286-6916 Jeannette Plante, GSFC, 301-902-4310 Bob Graber, JPL
Proposing Center:	GSFC
Participating Center(s):	JPL
Status:	X New: On going:
Performance Periods:	FY 00 – FY02
Benefits:	Stacked memories have been an enabling technology for solid state recorders and other applications requiring very large memory space. Projects that have used them are HST and LandSat. The X-2000 and the Nanosat projects are also designing stacked parts. This project benefits projects that depend on miniaturization in the near term like X.2000 and Nanosat but ultimately serves the entire electronics community by providing compact, reliable systems. Miniaturization has enabled portable technologies such as cellular phones and pocket-sized computers. Significant cost savings and an expansion of functionality can be realized on spacecraft and in airplanes when the electronics size is reduced. CNES and ESA are currently running tests on the 3D+ product and are very interested in our expanding this testing to make it comprehensive and as close to a full flight qualification as possible. ESA has agreed to allow 3D+ to sell small samples of the 10-layered test vehicle to NASA GSFC for testing without the burden of shared NRE costs, because the timing is very complementary to the testing they are doing. This funds leveraging is only available since ESA and CNES are involved at this time and will not be available if this work is done two years from now.
Partnerships and Endorsements	The leveraging will be achieved through the use of data and parts from ESA and CNES and the Nanosat project, respectively. Partnering will be with JPL for establishing the test plan based on assessment of the data accumulated to date. GSFC will procure the parts and perform the testing. Endorsement for this work has been received from the Nanosat project at GSFC.
Objectives of Proposal Activity:	The objective of this task is to evaluate electronic parts, which form a multichip module by virtue of being stacked one layer on top of another. This approach is being used by several manufacturers to provide small form factors and bring down the cost of the hardware (specifically with respect to mass memory). Most of these part types have not been evaluated for use in flight hardware though have the potential for improving its footprint and reliability. The 3D+ product and a product being developed by the Nanosat project, will be the first items to be evaluated under this task.
Technical Approach:	- Publish CNES and ESA data on stacked technologies on GSFC and JPL websites - Establish and coordinate test plan for 3D+ product and Nanosat Stacks - Coordinate use of existing and fabrication of new test fixtures and software - Procure test parts (define them if necessary) - Perform testing - Data Analysis and Coordination - Publish results

- Extend the same evaluation strategy to Irvine and DensePac product (and/or other parts).

Deliverable and Milestones:

Schedule:

- Web site updates (GSFC & JPL) 2QTR00, 01, 02
- Trip Report (GSFC) 2QTR00, 01, 02
- Test Plan (GSFC & JPL) 3QTR00, 01, 02
- DUT description (GSFC) 3QTR00, 01, 02
- Test Report (GSFC) 1QTR01, 01, 02